CLAIMS

What is claimed is:

1. A multi-chip electronic package comprising:

an organic, laminate chip carrier including a plurality of electrically conductive planes spacedly positioned therein and separated by respective layers of dielectric material, said chip carrier including a plurality of electrical contacts on a first surface thereof and a plurality of electrical conductors on a second surface thereof, selected ones of said electrical contacts being electrically coupled to selected ones of said electrical conductors; and

first and second semiconductor chips positioned on said first surface of said organic, laminate chip carrier in a stacked orientation, each semiconductor chip electrically coupled to selected ones of said electrical contacts.

2. The package of claim 1 wherein selected ones of said electrical contacts are electrically coupled to other selected ones of said electrical contacts such that selected ones of said semiconductor chips are electrically coupled to one another.

3. The package of claim 1 wherein said first semiconductor chip is directly positioned on said first surface of said organic, laminate chip carrier and said second semiconductor chip is positioned on said first semiconductor chip.

4. The package of claim 3 wherein said first semiconductor chip is an ASIC semiconductor chip and said second semiconductor chip is a memory chip.

5. The package of claim 4 wherein said first semiconductor chip is electrically coupled to selected ones of said electrical contacts by a plurality of solder balls.

6. The package of claim 4 wherein said second semiconductor chip is electrically coupled to selected ones of said electrical contacts by a plurality of wirebond connections.

7. The package of claim 6 further including a heat-sinking member positioned substantially over said first and second semiconductor chips.

8. The package of claim 7 further including a stiffener member positioned on said first surface of said organic, laminate chip carrier and spacedly positioned about said first and second semiconductor chips, said heat sinking member being positioned on said stiffener member.

9. The package of claim 1 further including a quantity of encapsulant material located on said first surface of said organic, laminate chip carrier and substantially covering both said first and second semiconductor chips.

10. The package of claim 1 wherein said organic, laminate chip carrier includes a thermally conductive member therein and a plurality of solder elements electrically coupling said first semiconductor chip to selected ones of said electrical contacts on said first surface of said organic, laminate chip carrier, said thermally conductive layer having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said electrical couplings formed by said solder elements on said selected ones of said electrical contacts.

11. The package of claim 10 wherein said thermally conductive member is comprised of a first layer of copper, a second layer of an iron alloy and a third layer of copper.

12. The package of claim 1 wherein said organic, laminate chip carrier includes a first multilayered portion including at least one dielectric layer and at least one conductive plane wherein said conductive plane includes signal lines capable of having signals pass therealong at a first frequency and a second multilayered portion bonded to said first multilayered portion and adapted for having said first and second semiconductor chips coupled thereto, said second multilayered portion including at least one dielectric layer and at least one conductive signal plane wherein said conductive signal plane of said second multilayered portion includes signal lines capable of having signals pass therealong at a higher frequency than said first frequency to thereby provide a high speed connection between said plurality of semiconductor devices.

13. The package of claim 12 wherein said second multilayered portion includes a conducting plane, first and second dielectric layers on opposite sides of said conducting plane, and the number of conductive signal planes is two, each conductive signal plane including said signal lines capable of having signals pass therealong and being positioned on a respective one of said first and second dielectric layers opposite said conducting plane.

14. The package of claim 13 wherein said second multilayered portion further includes a conductive through hole interconnecting at least one of said signal lines of said conductive signal plane on said first dielectric layer with at least one of said signal lines of said conductive signal plane on said second dielectric layer.

15. The package of claim 1 wherein said organic, laminate chip carrier includes an internal capacitor therein.

16. A method of making a multi-chip electronic package comprising:

providing an organic, laminate chip carrier having first and second surfaces and including a plurality of electrically conductive planes spacedly positioned therein and separated by respective layers of dielectric material;

providing a plurality of electrical contacts on said first surface of said organic, laminate chip carrier;

providing a plurality of electrical conductors on said second surface of said organic, laminate chip carrier, selected ones of said electrical contacts being electrically coupled to selected ones of said electrical conductors; and

positioning first and second semiconductor chips on said first surface of said organic, laminate chip carrier in a stacked orientation and electrically coupling said first and second semiconductor chips to said selected ones of said electrical contacts.

17. The method of claim 16 wherein electrically coupling of said first semiconductor chip is achieved using a plurality of solder members.

18. The method of claim 16 wherein electrically coupling of said second semiconductor chip is achieved using a plurality of wirebond connections.

19. The method of claim 16 further including electrically coupling a plurality of solder members to said selected ones of said electrical conductors, said solder members adapted for electrically coupling said selected ones of said electrical conductors to respective conductors on a circuitized substrate.

20. A multi-chip electronic package assembly including:

a circuitized substrate including a plurality of electrically conductive members thereon;

an organic, laminate chip carrier including a plurality of electrically conductive planes spacedly positioned therein and separated by respective layers of dielectric material, said chip carrier including a plurality of electrical contacts on a first surface thereof and a plurality of electrical conductors on a second surface thereof, selected ones of said

electrical contacts being electrically coupled to selected ones of said electrical conductors;

first and second semiconductor chips spacedly positioned on said first surface of said organic, laminate chip carrier in a stacked orientation and electrically coupled to selected ones of said electrical contacts; and

a plurality of electrically conductive elements electrically connecting said selected ones of said electrical conductors on said second surface of said organic, laminate chip carrier to respective ones of said electrically conductive members on said circuitized substrate.

21. The assembly of claim 20 wherein said circuitized substrate is a printed circuit board.

22. The assembly of claim 20 wherein said plurality of electrically conductive elements comprises a plurality of solder members.

23. The assembly of claim 20 further including a first plurality of solder members electrically coupling said first semiconductor chip to selected ones of said plurality of electrical contacts on said first surface of said laminate chip carrier.

24. The assembly of claim 23 further including a plurality of wirebond connections electrically coupling said second semiconductor chip to other selected ones of said plurality of electrical contacts on said first surface of said laminate chip carrier.